



# UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
Address: COMMISSIONER FOR PATENTS  
P.O. Box 1450  
Alexandria, Virginia 22313-1450  
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/825,714	04/14/2004	Jae-Deok Park	12576/4141	9210

7590 04/18/2006

Brinks Hofer Gilson & Lione  
Post Office Box 10395  
Chicago, IL 60610

EXAMINER


DUONG, TAI V

ART UNIT PAPER NUMBER

2871

DATE MAILED: 04/18/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	<b>Application No.</b>	<b>Applicant(s)</b>	
	10/825,714	PARK ET AL. 	
	<b>Examiner</b>	<b>Art Unit</b>	
	Tai Duong	2871	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 06 February 2006.
- 2a) ☐ This action is FINAL.                      2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-84 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 16-41 and 56-84 is/are allowed.
- 6) ☒ Claim(s) 1,4,5,8,9,13-15,42,45,46,49 and 53-55 is/are rejected.
- 7) ☒ Claim(s) 2,3,6,7,10-12,43,44,47,48 and 50-52 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 4/14/04 and 2/6/06 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All    b) ☐ Some \*    c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |   |   |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)             | 4) <input type="checkbox"/> Interview Summary (PTO-413)                     |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)    | Paper No(s)/Mail Date. _____  |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| Paper No(s)/Mail Date _____   | 6) <input type="checkbox"/> Other: _____                                    |

The election requirement of the last Office Action 01/11/06 is *withdrawn* in view of Applicant's remarks.

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1, 14, 15, 42, 54 and 55 are rejected under 35 U.S.C. 102(e) as being anticipated by Wen et al (US 2004/0239846).

Note Figs. 6, 11 and 14 which identically disclose the claimed transfective liquid crystal display and the method of forming an array substrate comprising each unit pixel including a plurality of sub-pixel regions (red, green and blue sub-pixel regions), each of the sub-pixel regions including a transmissive portion (250, 320, 420) and a reflective portion (240, 360, 410), the transmissive portions gathered together within each unit pixel; a thin film transistor in each sub-pixel region near a crossing of one of the gate and data lines adjacent to the sub-pixel region; a passivation layer (*not* labeled in Fig. 14) covering the thin film transistors and the gate and data lines, the passivation layer having openings that correspond to the transmissive portions in the unit pixels; a reflector formed over the passivation layer in each sub-pixel region, the reflector corresponding in position to the reflective portion; a pixel electrode in each sub-pixel

Art Unit: 2871

region, the pixel electrode contacting the thin film transistor through a contact hole (405, 406) in the passivation layer (paragraphs 0005, 0018, 0020 and 0021).

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 4, 5, 8, 9, 13, 45, 46, 49 and 53 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wen et al'846 in view of Park et al (US 2002/0109811).

As to claims 4, 8, 45 and 49, the only differences between the transfective liquid crystal display and the method of forming an array substrate of Wen et al and those of the instant claims are the amorphous silicon active layer and polysilicon active layer . Park et al disclose that it was known to employ in a transfective LCD either amorphous silicon active layer (element 134 of Figs. 10 and 11) or polysilicon active layer (element 166 of Figs. 12 and 13). Thus, it would have been obvious to a person of ordinary skill in the art in view of Park et al to employ in the LCD and method of Wen et al the amorphous silicon active layer for applications in LCD of large array area due to production yield and processing time (as compared with the polysilicon active layer). Also, it would have been obvious to a person of ordinary skill in the art in view of Park et al to employ in the LCD and method of Wen et al the polysilicon active layer for applications in high resolution LCD (as compared with the amorphous silicon active layer).

As to claims 5, 9 and 46, the only difference between the transfective liquid crystal display and the method of forming an array substrate of Wen et al and those of the instant claims is storage lines that are parallel with the gate lines and disposed between the sub-pixel regions. Park et al disclose in Fig. 12 disclose that it was known to employ storage lines 172 that are parallel with the gate lines and disposed between the pixel regions. Thus, it would have been obvious to a person of ordinary skill in the art in view of Park et al to employ in the LCD and method of Wen et al storage lines that are parallel with the gate lines and disposed between the sub-pixel regions for increasing the relaxation time of the liquid crystal layer.

As to claims 13 and 53, the only difference between the transfective liquid crystal display and the method of forming an array substrate of Wen et al and those of the instant claims is a color filter substrate that includes a black matrix 16 on a substrate, the black matrix corresponding to the thin film transistors and the gate and data lines; a color filter layer 18 on the substrate to cover the black matrix, the color filter layer having red, green and blue colors that corresponds to the sub-pixel regions; and a common electrode 13 on the color filter layer. Park et al disclose in Fig. 1 disclose that it was known to employ a color filter substrate that includes a black matrix on a substrate, the black matrix corresponding to the thin film transistors and the gate and data lines; a color filter layer on the substrate to cover the black matrix, the color filter layer having red, green and blue colors that corresponds to the sub-pixel regions; and a common electrode on the color filter layer. Thus, it would have been obvious to a person of ordinary skill in the art in view of Park et al to employ in the LCD and method of Wen et

Art Unit: 2871

al a color filter substrate that includes a black matrix on a substrate, the black matrix corresponding to the thin film transistors and the gate and data lines; a color filter layer on the substrate to cover the black matrix, the color filter layer having red, green and blue colors that corresponds to the sub-pixel regions; and a common electrode on the color filter layer for obtaining a full color transfective LCD with good contrast.

Claims 2, 3, 6, 7, 10-12, 43, 44, 47, 48 and 50-52 objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claims 2, 3, 6, 7, 10-12, 43, 44, 47, 48 and 50-52 are allowed over the prior art because none of the prior art discloses or suggests a transfective liquid crystal display and the method of forming an array substrate having the **combination** of the features recited in claim 1 or 42 with the features recited in claims 2, 3, 6, 7, 10-12, 43, 44, 47, 48 and 50-52.

Claims 16-41 and 56-84 are allowed over the prior art of record.

Claim 16 is allowed because none of the prior art discloses or suggests a method of forming an array substrate in a transfective liquid crystal display comprising the following steps: forming an active layer and an ohmic contact layer in series over each of the gate electrodes on the gate insulating layer; forming a plurality of data lines, a plurality of source electrodes, and a plurality of drain electrodes over the gate insulating layer, each of the source and drain electrodes contacting the ohmic contact layer, the data lines perpendicularly crossing the gate lines to define unit pixels, each of the unit

pixels including a plurality of sub-pixel regions, each sub-pixel region including a transmissive portion and a reflective portion, and the reflective portions of the sub-pixel regions gathered together in a center of each unit pixel; forming a first passivation layer on the gate insulating layer to cover the data lines, the source electrodes and the drain electrodes, the first passivation layer including, in each unit pixel, a contact hole exposing a portion of the drain electrode and a first opening exposing the gate insulating layer in the transmissive portions; forming reflectors within the reflective portions, each reflector corresponding to each sub-pixel region; forming a second passivation layer on the first passivation layer to cover the reflectors, the second passivation layer having a second opening exposing the gate insulating layer in the transmissive portions; forming pixel electrodes on the second passivation layer in the sub-pixel regions. Claims 17-28 are also allowed since they depend on claim 16.

Claim 29 is allowed because none of the prior art discloses or suggests a method of forming an array substrate in a transflective liquid crystal display comprising the following steps: forming the reflective portions of the sub-pixel regions gathered together in a center of each unit pixel; forming a buffer layer on the entire substrate; forming a plurality of polycrystalline silicon layers and a plurality of polysilicon patterns, the polycrystalline silicon layers disposed near corners of the unit pixels, the polysilicon patterns disposed between the sub-pixel regions; forming a gate insulating layer on the buffer layer to cover the polycrystalline silicon layers and the polysilicon patterns; forming a plurality of gate lines, a plurality of storage lines, and a plurality of gate electrodes on the gate insulating layer; forming a first passivation layer on the gate

Art Unit: 2871

insulation layer to cover the gate lines, the storage lines and the gate electrodes, the first passivation layer and the gate insulating layers having contact holes exposing portions of the polycrystalline silicon layers; forming a plurality of data lines, a plurality of source electrodes, and a plurality of drain electrodes on the first passivation layer, each of the source and drain electrodes contacting the polycrystalline silicon layer through the contact holes, the data lines perpendicularly crossing the gate lines to define the unit pixels; forming second and third passivation layers in series on the first passivation layer to cover the data lines, the source electrodes and the drain electrodes, the second and third passivation layers including in each unit pixel a first contact hole exposing a portion of the drain electrode and a first opening exposing the first passivation layer in the transmissive portions; forming reflectors within the reflective portions, each reflector corresponding to each sub-pixel region; forming a fourth passivation layer on the third passivation layer to cover the reflectors, the second passivation layer in each unit pixel having a second contact hole exposing the portion of the drain electrode; forming pixel electrodes on the fourth passivation layer in the sub-pixel regions, each pixel electrode contacting the drain electrode through the second contact hole. Claims 30-41 are also allowed since they depend on claim 29.

Claim 56 is allowed because none of the prior art discloses or suggests a transfective liquid crystal display comprising each unit pixel including a plurality of sub-pixel regions, each of the sub-pixel regions including a reflective portion containing a reflector and a transmissive portion, adjacent pairs of the transmissive portions in different sub-pixel regions within each unit pixel arranged such that no reflective portion



Art Unit: 2871

is disposed between the pair of transmissive portions, wherein the transmissive portion is devoid of the reflector. Claims 57-68 are also allowed since they depend on claim 56.

Claim 69 is allowed because none of the prior art discloses or suggests a transfective liquid crystal display comprising each unit pixel including a plurality of sub-pixel regions, each of the sub-pixel regions including a transmissive portion, a reflective portion, a border area between the transmissive and reflective portions, a reflector and a passivation layer, the passivation layer and reflector disposed in the reflective portion and terminating in the border area before reaching the transmissive portion such that the border area contains a disclination of the passivation area and reflector that has a slope oblique to the first and second substrates, wherein the border area and reflective portion of at least one sub-pixel region in each unit pixel does not completely encircle the transmissive portion of the at least one sub-pixel region. Claims 70-84 are also allowed since they depend on claim 69.

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Chen et al disclose a transfective LCD having two TFTs each connected to the reflective and transmissive regions.

Any inquiry concerning this communication should be directed to Tai Duong at telephone number (571) 272-2291.

The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

TD

04/06

TAMTONG  
PATENT EXAMINER